

### VC mapping

Virtual channel A: (2, 7, 5)

Virtual channel B: (1)

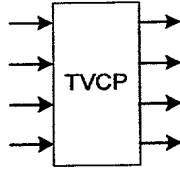
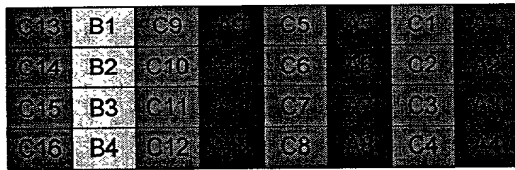
Virtual channel C: (3, 4, 6, 8)

Datapath width = 4 bytes

Number of STS-1 timeslots = 8

### System Side

Per-VC data words



### Line Side

Timeslot-interleaved data words

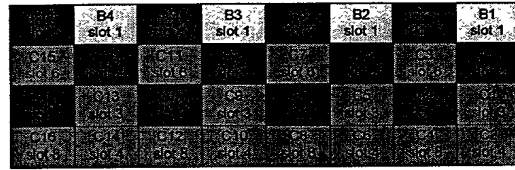


Figure 1: Example of virtual concatenation

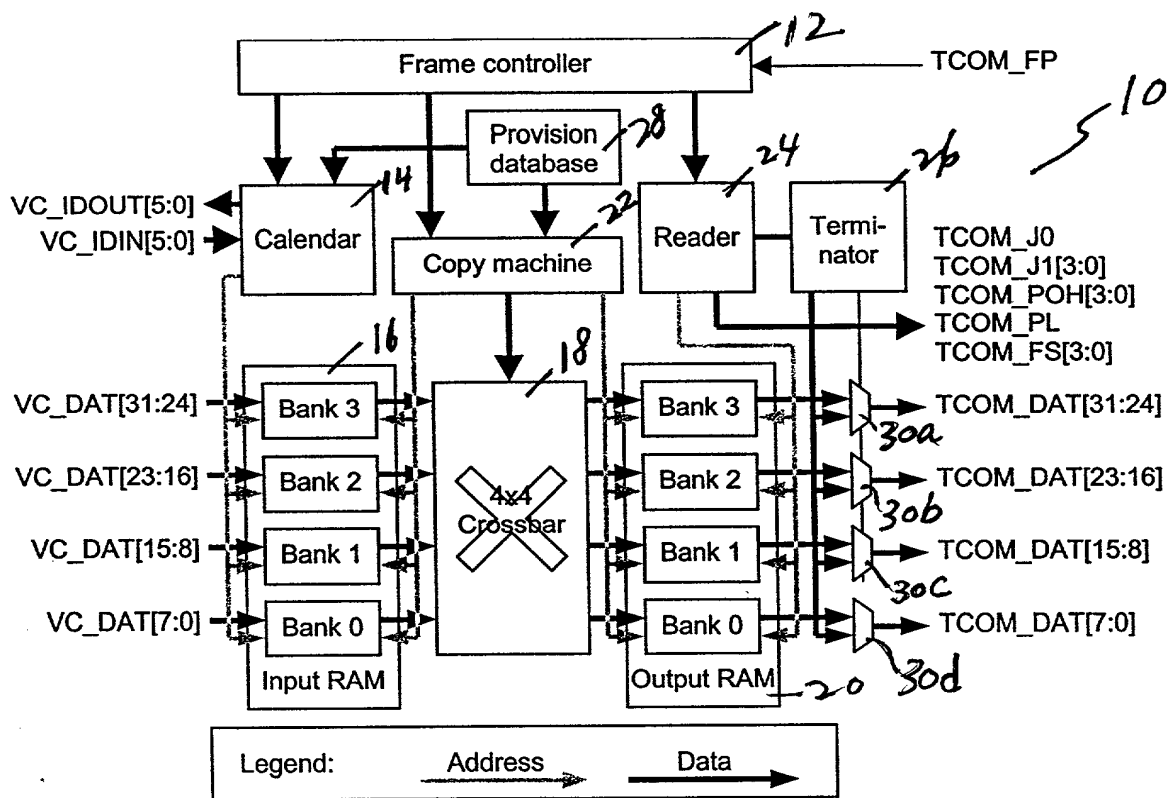


Figure 2: Block diagram of TVCP-48

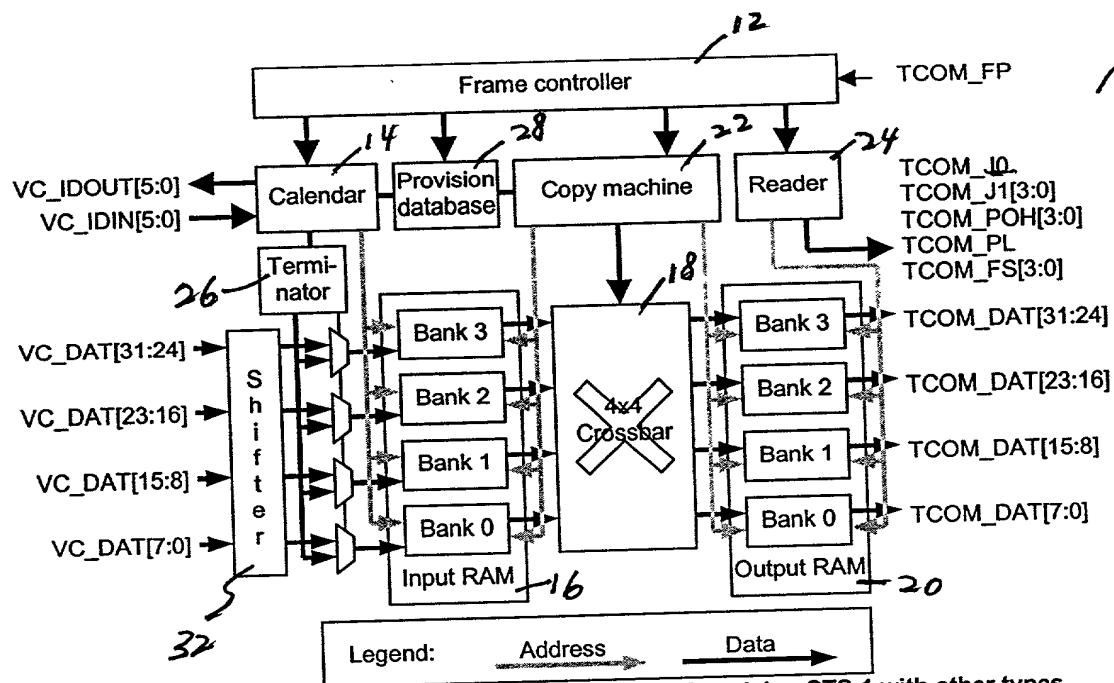


Figure 3: Block diagram of TVCP-48 with support for mixing STS-1 with other types

Fig. 4a

Example Channel Mapping

Channel	0	1	2
Bandwidth	STS-1-1v	STS-1-2v	STS-1-3v
Timeslot	4	1 5	3 0 2
Sequence Number	0	0 1	0 1 2

Fig. 4b

Example Calendar and Sequence Number Setting

Timeslot	0	1	2	3	4	5
Channel	1	2	0	1	2	2
Sequence Number	1	0	2	0	0	1

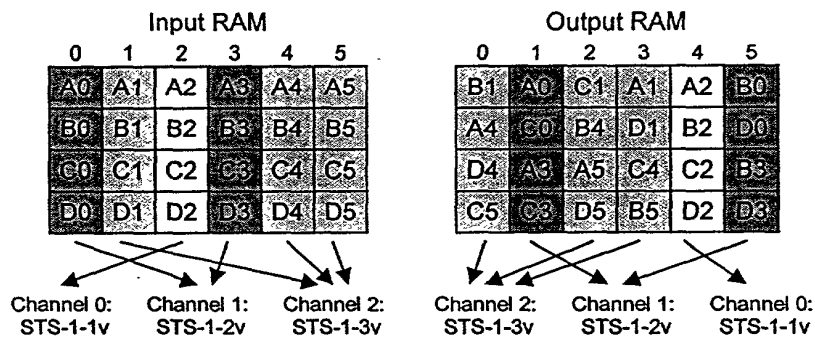
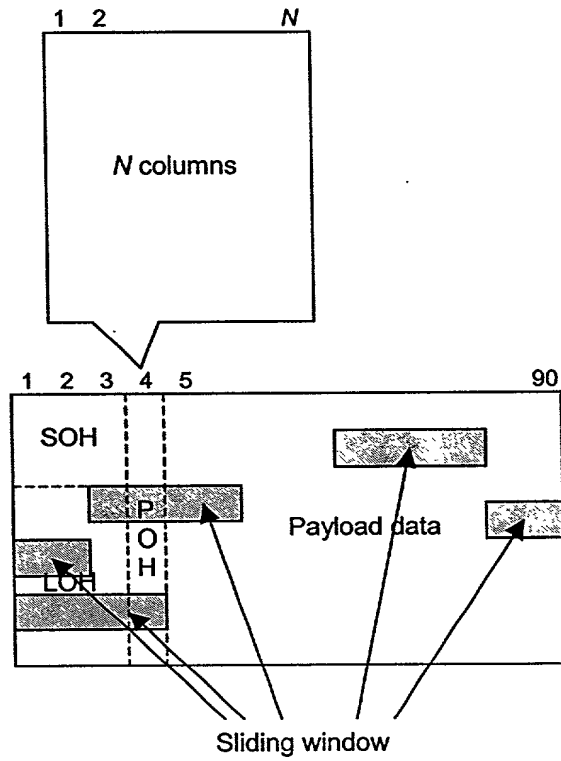


Fig 4C : Footprint of Data Bytes in Input RAM and Output RAM

### Figure 5. Data Movement from Input RAM to Output RAM



**Figure 6** Sliding Window Across a SONET/SDH Frame



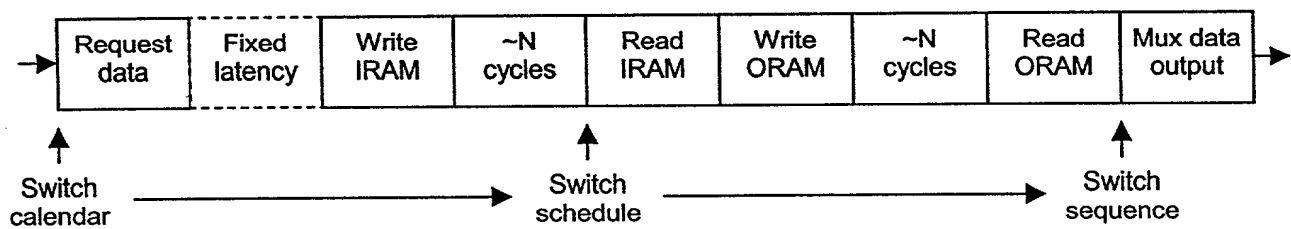
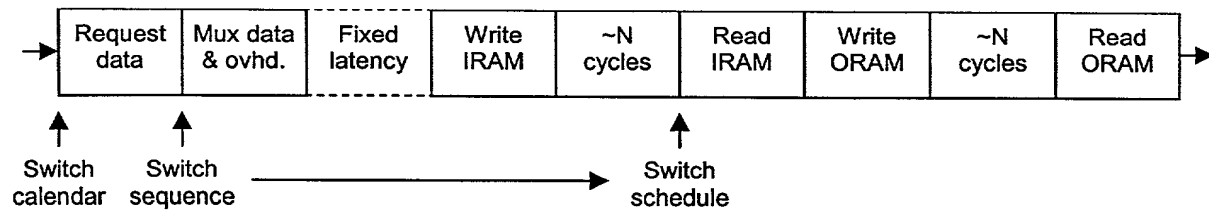


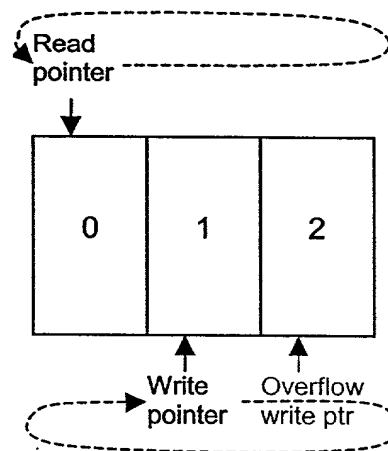
Fig. 8 : Pipeline Stages of the TVCP Datapath





**Figure 9. Pipeline Stages of the TVCP Datapath for Early Overhead Insertion**

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**Fig. 10: Triple Buffer in Input RAM**